IN THE CLAIMS:

All pending claims are set forth below. Cancelled and withdrawn claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (previously amended), (cancelled), (withdrawn), (new), (previously added), (reinstated - formerly claim #), (previously reinstated), (re-presented - formerly dependent claim #), or (previously re-presented).

Please AMEND claims 1-16 and 18-25 and ADD new claims 27-40 in accordance with the following:

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1. (currently amended) Digital circuitry, operative repetitively to perform a series of processing cycles, comprising:

an input signal processing circuit performing ~~means operable,~~ in each cycle, ~~to perform~~ a predetermined processing operation on one or more input ~~signals~~ signal(s) received by the digital circuitry to derive therefrom one or more first ~~signals~~ signal(s), said predetermined processing operation being commenced in response to a first clock signal;

a first clocked ~~means switchable, by application thereto of~~ element receiving said one or more first signal(s) and a second clock signal, and producing one or more second signal(s), said first clocked element being switchable by said second clock signal between a first responsive state, in which the first clocked ~~means are operable~~ element changes said one or more second signal(s) in response to a change in said one or more ~~the~~ first signal(s) [~~to change one or more second signals produced thereby~~, and a first non-responsive state in which no change in said one or more ~~the~~ second signal(s) occurs;

a second clocked ~~means switchable, by application thereto of~~ element receiving said one or more second signal(s) and a third clock signal, and producing one or more output signal(s) of said digital circuitry, said second clocked element being switchable by said third clock signal between a second responsive state, in which the second clocked element changes said one or more output signal(s) ~~means are operable~~ in response to a change in said one or more ~~the~~ second signal(s) ~~to change one or more output signals of the circuitry~~, and a second non-responsive state in which no change in said one or more ~~the~~ output signal(s) occurs; and

clock generating ~~means for deriving~~ circuitry generating the second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a preselected delay time and said third clock signal being delayed relative to the first clock signal by less than said preselected delay time such that in each cycle the first clocked element ~~means~~ enters said first non-responsive state before the end of said

predetermined processing operation, and said second clocked element ~~means~~ enters said second responsive state when the first clocked element is ~~means are~~ in said first non-responsive state.

2. (currently amended) Digital circuitry as claimed in claim 1, wherein said third clock signal has ~~no or~~ no substantial delay relative to said first clock signal.

3. (currently amended) Digital circuitry as claimed in claim 1, wherein said preselected delay time is chosen such that said first clocked element ~~means~~ enters said first non-responsive state at least a predetermined hold time before ~~the~~ an end of said predetermined processing operation, which predetermined hold time is the minimum period for which the ~~or each~~ one or more first ~~signal~~ signal(s) must remain stable after the first clocked element ~~means~~ enters said first non-responsive state.

4. (currently amended) Digital circuitry as claimed in claim 1, wherein ~~said clock generating means are such that~~ a predetermined enabling change in said generated third clock signal ~~which change causes~~ enabling the second clocked element ~~means~~ to change from said second non-responsive state to said second responsive state, and said predetermined enabling change occurs substantially simultaneously with ~~one of the changes~~ a first change in said first clock signal.

5. (currently amended) Digital circuitry as claimed in claim 4, wherein said ~~one~~ first change in the first clock signal is a predetermined enabling change ~~in that signal which causes~~ enabling said predetermined processing operation to commence.

6. (currently amended) Digital circuitry as claimed in claim 4, wherein a predetermined disabling change in the third clock signal, ~~which change causes~~ enabling the second clocked element ~~means~~ to change from said second responsive state to said second non-responsive state, is delayed ~~substantially~~ relative to ~~one of the changes~~ a second change in the first clock signal.

7. (currently amended) Digital circuitry as claimed in claim 6, wherein the clock generating circuitry comprises ~~means include~~:

a delay element ~~means for~~ delaying the first clock signal to produce a delayed version thereof; and

a logic element ~~means for~~ logically combining the first clock signal with ~~said~~ a delayed version thereof such that said enabling change in the third clock signal [~~is~~]

occurs substantially ~~simultaneous~~ simultaneously with said enabling change in said first clock signal, and said disabling change in the third clock signal [~~is~~] occurs substantially ~~simultaneous~~ simultaneously with ~~one of the changes~~ a change in said delayed version of the first clock signal.

8. (currently amended) Digital circuitry as claimed in claim 7, wherein said clock generating circuitry ~~means~~ further comprises:

a include delay balancing element ~~means~~ connected between said delay element ~~means~~ and said first clocked element ~~means for~~ receiving said delayed version of the first clock signal and ~~for~~ deriving therefrom said second clock signal;~~,~~

the delay balancing element ~~means~~ having a first propagation delay between said ~~one~~ change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal that causes the first clocked element ~~means~~ to change from said first non-responsive state to said first responsive state;~~,~~

said logic element having ~~said first propagation delay being substantially equal to~~ a second propagation delay~~, of said logic means~~ between said ~~one~~ change in said delayed version of the first clock signal and said disabling change in the third clock signal;~~.~~ and

said first propagation delay being substantially equal to said second propagation delay.

9. (currently amended) Digital circuitry as claimed in claim 1, wherein said input signal processing circuit comprises:

a ~~means include further~~ third clocked element receiving said one or more input signal(s) ~~means switchable, by application thereto of~~ and said first clock signal, and producing one or more basic clock signal(s), said third clocked element being switchable by said first clock signal~~,~~ between a third responsive state, in which said ~~further~~ third clocked element changes said one or more basic clock signal(s) ~~means are operable~~] in response to a change in said one or more input signal(s) [~~to change one or more basic signals produced thereby~~, and a third non-responsive state in which no change in said one or more ~~the~~ basic clock signal(s) occurs; and

signal processing circuitry processing ~~means for deriving~~ said one or more first ~~signals~~ signal(s) from said one or more ~~the~~ changed and unchanged basic clock signal(s).

10. (currently amended) Digital circuitry as claimed in claim 1, wherein said first clocked element comprises ~~means include~~ a D-type latch element.

11. (currently amended) Digital circuitry as claimed in claim 1, wherein said second clocked element comprises ~~means include~~ a transparent half-latch element.

12. (currently amended) Digital circuitry as claimed in claim 1, wherein at least one of said one or more first ~~signals~~ signal(s) ~~and/or~~ and said one or more second ~~signals~~ signal(s), said one or more first signal(s) ~~and/or said third signals and/or~~ and said one or more output ~~signals~~ signal(s), and said one or more second signal(s) and said one or more output signal(s) ~~are~~ is/are a complementary signal ~~pairs~~ pair.

13. (currently amended) Digital circuitry as claimed in claim 1, wherein the or each at least one of the said one or more first ~~signal~~ signal(s) ~~and/or the or each~~, and said one or more second ~~signal~~ signal(s) ~~and/or the or each third signal and/or the or each~~ , and said one or more output ~~signal~~ signal(s) is a thermometer-coded signal.

14. (currently amended) Digital circuitry as claimed in claim 1, further including power supply ~~means for supplying~~ circuitry supplying power to said second clocked element ~~means~~ independently from that supplied to at least another part of said digital circuitry.

15. (currently amended) Digital circuitry as claimed in claim 1, including a plurality of individual circuit units, each circuit unit including such an input signal processing circuit ~~means~~ and such a first clocked element ~~means~~ and such a second clocked element ~~means~~.

16. (currently amended) Digital circuitry as claimed in claim 15, wherein the clock generating circuitry comprises ~~means include~~:

a global clock generator provided in common for all said circuit units and operable to produce a basic clock signal; and

a plurality of local clock drivers, each said local clock driver corresponding to one or more of said circuit unit(s), and each said local clock driver being connected to the global clock generator for receiving therefrom said basic clock signal and being operable to derive therefrom said ~~a unique such~~ third clock signal for application to said second clocked circuit ~~means~~ in ~~the or~~ each of its said one or more corresponding circuit ~~units~~ unit(s).

17. (original) Digital circuitry as claimed in claim 16, wherein each said circuit unit has its own individually-corresponding one of said local clock drivers.

18. (currently amended) Digital circuitry as claimed in claim 16, wherein said

global clock generator is operable to produce said basic clock signal and a complementary basic clock signal ~~respective mutually-complementary~~, wherein both said basic clock signal and said complementary ~~such~~ basic clock signals ~~which~~ are applied in common to all of said local clock drivers of said plurality.

19. (currently amended) Digital circuitry as claimed in claim 15, having at least two power supplies for the plurality of circuit units, each said power supply corresponding to one or more of said circuit unit(s) and supplying power to a predetermined part of its said one or more corresponding circuit unit(s), said digital circuitry further comprising a power supply decoupling circuit decoupling ~~means for decoupling~~ said at least two power supplies from one another ~~the respective power supplies of respective predetermined parts of at least two different circuit units of said plurality~~.

20. (currently amended) Digital circuitry as claimed in claim 19, wherein each said circuit unit has its own individually-corresponding one of said at least two power supplies, and said power supply decoupling circuit ~~means are operable to~~ decouples the power supply of said ~~such a~~ predetermined part of each said circuit unit from that of each other one of the one or more circuit unit(s).

21. (currently amended) Digital circuitry as claimed in claim 19, wherein said predetermined part of said circuit unit includes said second clocked element ~~means~~.

22. (currently amended) Digital circuitry as claimed in claim 17, having at least two power supplies for the plurality of circuit units, each said power supply corresponding to one or more of said circuit unit(s) and supplying power to a predetermined part of its said one or more corresponding circuit unit(s), said digital circuitry further comprising:

a power supply decoupling circuit decouplings ~~means for decoupling~~ said at least two power supplies from one another ~~the respective power supplies of respective predetermined parts of at least two different circuit units of said plurality~~;

wherein said predetermined part of said circuit unit includes said second clocked element ~~means~~ and said local clock driver of the circuit unit.

23. (currently amended) Mixed-signal circuitry, including:

digital circuitry, operative repetitively to perform a series of processing cycles, comprising:

an input signal processing circuit performing ~~means operable~~, in each cycle, ~~to perform~~ a predetermined processing operation on one or more input ~~signals~~

signal(s) received by the digital circuitry to derive therefrom one or more first ~~signals~~ signal(s), said predetermined processing operation being commenced in response to a first clock signal[~~;~~],

a first clocked element receiving said one or more first signal(s) and ~~means switchable, by application thereto of~~ a second clock signal, and producing one or more second signal(s), said first clocked element being switchable by said second clock signal between a first responsive state, in which the first clocked element changes said one or more second signal(s) ~~means are operable~~ in response to a change in said one or more ~~the~~ first signal(s) ~~to change one or more second signals produced thereby~~, and a first non-responsive state in which no change in said one or more ~~the~~ second signal(s) occurs~~;~~,

a second clocked element receiving said one or more second signal(s) and ~~means switchable, by application thereto of~~ a third clock signal, and producing one or more output signal(s) of said digital circuitry, said second clocked element being switchable by said third clock signal ~~,~~ between a second responsive state, in which the second clocked element changes said one or more output signal(s) ~~means are operable~~ in response to a change in said one or more ~~the~~ second signal(s) to change one or more output ~~signals~~ signal(s) of the circuitry, and a second non-responsive state in which no change in said one or more ~~the~~ output signal(s) occurs~~;~~, and

clock generating circuitry generating ~~means for deriving~~ the second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a preselected delay time and said third clock signal being delayed relative to the first clock signal by less than said preselected delay time such that in each cycle the first clocked element ~~means~~ enters said first non-responsive state before the end of said predetermined processing operation, and said second clocked element ~~means~~ enters said second responsive state when the first clocked element is ~~means are~~ in said first non-responsive state; and

analog circuitry connected to said digital circuitry for receiving therefrom said one or more output ~~signals~~ signal(s) and operable to produce one or more analog ~~signals~~ signal(s) in dependence upon the received one or more output signal(s).

24. (original) Mixed-signal circuitry as claimed in claim 23, including a digital-to-analog converter.

25. (currently amended) Mixed-signal circuitry as claimed in claim 23, wherein the analog circuitry further comprises~~;~~ ~~includes~~

a plurality of current sources or current sinks sourcing or sinking respective

currents, and a plurality of switch circuits, connected to the plurality of current ~~sources/sinks~~ sources or current sinks switching said currents selectively ~~for performing predetermined switching operations~~ in dependence upon said one or more output signal(s) so as to produce said one or more analog ~~signals~~ signal(s).

26. (currently amended) Mixed-signal circuitry as claimed in claim 23, wherein said digital circuitry further comprises:

~~includes~~ power supply circuitry ~~means for~~ supplying power to ~~the second clocked means~~ a first part of said digital circuitry independently from that supplied to at least ~~another~~ a second part of said digital circuitry~~;~~, wherein said first part of said digital circuitry is the second clocked element, and

wherein said power supply circuitry ~~means are~~ also supplies ~~operable to supply~~ power to said analog circuitry independently of the power supplied to the or each said second clocked means first part and to said ~~other~~ second part of the digital circuitry.

27. (new) A digital circuit, comprising:

an input signal processing circuit clocked by a first clock signal, inputting one or more first signal(s), and performing a predetermined processing operation on the first signal(s);

a first latch circuit clocked by a second clock signal, and inputting an output signal from the input signal processing circuit;

a second latch circuit clocked by a third clock signal, and inputting an output signal from the first latch circuit; and

a clock generating circuit generating the second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a predetermined delay time, and a rising edge of the third clock signal occurring at substantially the same time as a rising edge of the first clock signal, and a falling edge of the third clock signal occurring at substantially the same time as a rising edge of the second clock signal.

28. (new) The digital circuit as claimed in claim 27, wherein the clock generating circuit comprises:

a delay element delaying the first clock signal to produce a delayed version thereof, and

a logic element logically combining the first clock signal with the delayed version thereof such that an enabling change in the third clock signal occurs substantially simultaneously with an enabling change in the first clock signal, and a disabling change in the third clock signal occurs substantially simultaneously with a change in the delayed version of the first clock signal.

29. (new) The digital circuit as claimed in claim 28, wherein said clock generating circuit further comprises:

a delay balancing element connected between said delay element and said first latch circuit receiving said delayed version of the first clock signal and deriving therefrom said second clock signal,

the delay balancing element having a first propagation delay between said change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal enabling the first latch circuit to change from a non-responsive state to a responsive state,

said logic element having a second propagation delay between said change in said delayed version of the first clock signal and said disabling change in the third clock signal, and

said first propagation delay being substantially equal to said second propagation delay.

30. (new) A digital circuit comprising:

an input signal processing circuit clocked by a first clock signal, inputting one or more first signal(s), and performing a predetermined processing operation on the first signal(s);

a first latch circuit clocked by a second clock signal, and inputting an output signal from the input signal processing circuit;

a second latch circuit clocked by a third clock signal, and inputting an output signal from the first latch circuit; and

a clock generating circuit generating the second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a predetermined delay time, and a rising edge of the third clock signal occurring substantially at a same time as a rising edge of the first clock signal and enabling the second latch circuit to enter a responsive state during a non-responsive state of the first latch circuit.

31. (new) The digital circuit as claimed in claim 30, wherein the clock generating circuit comprises:

a delay element delaying the first clock signal to produce a delayed version thereof, and

a logic element logically combining the first clock signal with a delayed version thereof such that an enabling change in the third clock signal occurs substantially simultaneously with an enabling change in the first clock signal, and a disabling change in the third clock signal occurs substantially simultaneously with a change in

the delayed version of the first clock signal.

32. (new) The digital circuit as claimed in claim 31, wherein said clock generating circuit further comprises:

a delay balancing element connected between said delay element and said first latch circuit receiving said delayed version of the first clock signal and deriving therefrom said second clock signal, and

the delay balancing element having a first propagation delay between said change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal causing the first latch circuit to change from a non-responsive state to a responsive state,

said logic element having a second propagation delay between said change in said delayed version of the first clock signal and said disabling change in the third clock signal, and

said first propagation delay being substantially equal to said second propagation delay.

33. (new) A digital-analog converter circuit, comprising:

a digital circuit, operative repetivtively to perform a series of processing cycles, comprising:

an input signal processing circuit clocked by a first clock signal, inputting one or more first signal(s), performing a predetermined processing operation of the one or more first signal(s), and outputting a first output signal,

a first latch circuit clocked by a second clock signal, inputting the first output signal, and outputting a second output signal,

a second latch circuit clocked by a third clock signal, and inputting the output signal from the first latch circuit, and

a clock generating circuit generating second and the third clock signals from the first clock signal,

the second clock signal being delayed relative to the first clock signal by a predetermined delay time, and a rising edge of the third clock signal edge occurring at substantially the same time as a rising edge of the first clock signal and a falling edge of the third clock signal occurring at substantially the same time as a rising edge of the second clock signal; and

an analog circuit connected to said digital ciruit receiving therefrom said one or more output signal(s) and operable to produce one or more analog signal(s) in dependence upon one or more output signal(s).

34. (new) The digital-analog converter circuit as claimed in claim 33, wherein the clock generating circuit comprises:

a delay element delaying the first clock signal to produce a delayed version thereof, and

a logic element logically combining the first clock signal with a delayed version thereof such that an enabling change in the third clock signal occurs substantially simultaneously with an enabling change in the first clock signal, and a disabling change in the third clock signal occurs substantially simultaneously with a change in the delayed version of the first clock signal.

35. (new) The digital-analog converter circuit as claimed in claim 34, wherein said clock generating circuit further comprises:

a delay balancing element connected between said delay element and said first clocked element receiving said delayed version of the first clock signal and deriving therefrom said second clock signal,

the delay balancing element having a first propagation delay between said change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal causing the first clocked element to change from a first non-responsive state to a first responsive state,

said logic element having a second propagation delay between said change in said delayed version of the first clock signal and said disabling change in the third clock signal, and

said first propagation delay being substantially equal to said second propagation delay.

36. (new) A digital-analog converter circuit, comprising:

a digital circuit to perform a series of processing cycles, comprising:

an input signal processing circuit clocked by a first clock signal, inputting one or more first signal(s), and performing a predetermined processing operation on the first signal(s), and outputting a first output signal,

a first latch circuit clocked by a second clock signal and inputting the first output signal,

a second latch circuit clocked by a third clock signal and inputting an output signal from the first latch circuit, and

a clock generating circuit generating the second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a predetermined delay time, a rising edge of the third clock signal without a

substantial delay time relative to a rising edge of the first clock signal or with a shorter delay time then the delay time of the second clock signal and making the second latch circuit enter a responsive state during a non-responsive state of the first latch circuit; and

an analog circuit connected to said digital circuit receiving therefrom said one or more output signal(s) to produce one or more analog signal(s) in dependence upon one or more output signal(s).

37. (new) The digital-analog converter circuit as claimed in claim 36, wherein the clock generating circuit comprises:

a delay element delaying the first clock signal to produce a delayed version thereof, and

a logic element logically combining the first clock signal with a delayed version thereof such that an enabling change in the third clock signal occurs substantially simultaneously with an enabling change in the first clock signal, and a disabling change in the third clock signal is substantially simultaneous with a change in the delayed version of the first clock signal.

38. (new) The digital-analog converter circuit as claimed in claim 37, wherein said clock generating circuit further comprises:

a delay balancing element connected between said delay element and said first clocked element for receiving said delayed version of the first clock signal and for deriving therefrom said second clock signal,

the delay balancing element having a first propagation delay between said change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal that causes the first clocked element to change from a first non-responsive state to a first responsive state,

said logic element having a second propagation delay between said change in said delayed version of the first clock signal and said disabling change in the third clock signal,

said first propagation delay being substantially equal to said second propagation delay.

39. (new) A digital circuit, comprising:

a digital input circuit receiving a plurality of digital signals in response to a first clock signal;

a delay element receiving the first clock signal and outputting a delayed clock signal;

a clock generating circuit receiving the first clock signal and generating a second clock signal, produced from the delayed clock signal, and a third clock signal, produced from the first clock signal and the delayed clock signal;

a first latch circuit, coupled to the digital input circuit, receiving the output signal from the digital input circuit in response to the second clock signal; and

a second latch circuit, coupled to the first latch circuit, receiving the output signal from the first latch circuit in response to the third clock signal.

40. (new) A digital-analog converter circuit, comprising:

a digital circuit performing a series of processing cycles, comprising:

a digital input circuit receiving a plurality of digital signals in response to a first clock signal,

a delay element receiving the first clock signal and outputting a delayed clock signal,

a clock generating circuit receiving the first clock signal and generating a second clock signal, produced from the delayed clock signal, and a third clock signal, produced from the first clock signal and the delayed clock signal,

a first latch circuit, coupled to the digital input circuit, receiving the output signal from the digital input circuit in response to the second clock signal, and

a second latch circuit, coupled to the first latch circuit, receiving the output signal from the first latch circuit in response to the third clock signal; and

an analog circuit connected to said digital circuit receiving therefrom said one or more output signal(s) producing one or more analog signal(s) in dependence upon one or more output signal(s).